Remarks:

Reconsideration of the application, as amended herein, is respectfully requested.

Claims 1 - 17 are presently pending in the application. Claims 1, 2 and 11 have been amended.

In item 6 of the above-identified Office Action, claims 1 - 10 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by U. S. Patent No. 5,678,003 to Brooks ("**BROOKS**"). In items 8, 12, 14, 16, 18 and 21 of the Office Action, claims 11, 12, 13, 14, 16 and 17 were rejected, respectively, under 35 U.S.C. § 102(b) as also allegedly being anticipated by U. S. Patent No. 5,678,003 to Brooks ("**BROOKS**")

In item 23 of the above-identified Office Action, claim 7 was rejected under 35 U.S.C. § 103(a) as allegedly being obvious over **BROOKS** in view of pages 658 - 659 of *Hennessy*, Computer Organization and Design: The Hardware/Software Interface, Morgan Kaufmann Publishers, 2nd edition ("**HENNESSY**"). In item 27 of the above-identified Office Action, claim 15 was also rejected under 35 U.S.C. § 103(a) as allegedly being obvious over **BROOKS** in view of **HENNESSY**.

Applicant respectfully traverses the above rejections, as applied to the amended claims.

First, Applicant incorporates the arguments of the previous response herein, in their entirety. Further, in order to more clearly point out the claimed invention, Applicant has amended claim 1 to recite, among other limitations:

> "other components connected to said stopping device, said stopping device **issuing a stop command** causing said other components to be stopped, in addition to stopping said program operation unit with which said stopping device is associated; and
>
> said other components including at least one further program operation unit or at least one peripheral, **said stopping command being selectively provided** from said stopping device to said other component **if said other component is said further program operation unit and said stop command being directly provided** from said stopping device to said other component **if said other component is a peripheral.**" [emphasis added by Applicant]

Applicant's claim 11 has been amended to recite, among other limitations:

> "peripherals connected to said stopping device, said stopping device **issuing a stop command directly to said peripherals** causing said peripherals to be stopped, in addition to stopping said program operation unit with which said stopping device is associated." [emphasis added by Applicant]

That Applicant's claimed "**stop command**" is supported on page 11, line 19 - page 12, line 26, wherein operation of Applicant's **On Chip** Debug Support (OCDS) modules are described as follows:

> "**The trigger for the first OCDS module OCDS1 to stop the first program running unit CORE1, the second**

program running unit CORE2 and the peripheral units P1 and P2 occurs when the first OCDS module OCDS1 finds that a breakpoint condition is satisfied by the first programming running unit CORE1. It is also possible (but not necessary) for the first OCDS module OCDS1 to stop the first peripheral unit P1 and the second peripheral unit P2 in the situation where the second OCDS module OCDS2 causes it to stop the first program running unit CORE1. It is preferably possible to use the first OCDS module OCDS1 to select whether this is the case.

The second program running unit CORE2 is stopped by the first OCDS module OCDS1 by a signal BRK1 which the first OCDS module OCDS1 emits to the second OCDS module OCDS2, and which the second OCDS module OCDS2 uses to stop the second program running unit CORE2. The first program running unit CORE1 is stopped by the second OCDS module OCDS2 by a signal BRK2 which the second OCDS module OCDS2 emits to the first OCDS module OCDS1, and which the first OCDS module OCDS1 uses to stop the first program running unit CORE1. For the sake of completeness, it should be mentioned that the signals BRK1 and BRK2 can also be supplied directly to the program running unit which they are intended to stop; this also makes it possible to stop program running units which have no associated OCDS module.

On their way to the OCDS modules for which they are intended, the signals BRK1 and BRK2 pass through the stopping configuration apparatus CONF. The stopping configuration apparatus CONF contains switching elements via which it is possible to select whether the signal BRK1 is passed on to the second OCDS module OCDS2, and/or whether the signal BRK2 is passed on to the first OCDS module OCDS1.

The peripheral units P1 and P2 are stopped by the first OCDS module OCDS1 emitting a signal SUSPEND = 1. The suspend signal SUSPEND is emitted, for example, at the time at which the program running units CORE1 and/or CORE2 are stopped, and is supplied to the stopping delay apparatus DEL. The stopping delay apparatus DEL passes the signal on, with a specific delay, to the peripheral units P1 and P2, and in consequence stops them. The delaying of passing on of the SUSPEND signal to the peripheral units P1 and P2 results in that they are not stopped until a certain amount of time has passed from the time at which the

> program running units were stopped." [emphasis added by Applicant]

As seen from the above quotation from the instant specification, the OCDS module (i.e., Applicant's claimed **stopping device**) affirmatively issues a BRK1 command to the second processor to stop the second processor, as well as, affirmatively issues a SUSPEND command directly to the peripherals, to stop the peripherals. See also, **SUSPEND** line and **BRK1** lines of Applicant's sole figure. As such, Applicant's claimed **stopping device** affirmatively issues a stop command to the other devices, both directly to the peripheral devices and **selectively** to the other processors.

As noted in the Office Action, in the **BROOKS** reference when a processor reaches an instruction address breakpoint, it will enter a restartable stop state **and assert the common stop pin**. As stated on page 4 of the Office Action, in connection with the **BROOKS** reference, it is stated:

> "After the processor asserts the stop pin, 112, the other processors stop program running. Each processor **then asserts a stop_req, which is detected by the interface tool.** When all of the processors have asserted a stop_req bit, **the interface tool issues a halt instruction to the bus arbiter, stopping all bus activity.** Therefore the stopping device associated with the processor that encountered the address breakpoint first causes the other components to be **stopped by asserting a stop pin**, which causes the other CPUs and the bus arbiter to stop. Since it was

> the stopping device that caused the chain reaction, it is responsible for stopping the system."

Assuming, arguendo, that, in **BROOKS**, the first processor that detects a breakpoint is analogous to Applicant's claimed **stopping device** because it "**asserts a stop_req**" that starts a chain reaction that is responsible for stopping the system, that processor still **doesn't issue a stop command "directly to" the peripherals**, as presently claimed by claim 11. Rather, it is the scan interface tool of **BROOKS** that communicates with the peripherals, and not the processor. See, Fig. 4 of **BROOKS** step 314 ("When each processor indicates a STOP_REQ, **the scan interface tool issues a JTAG HALT instruction to the system bus arbiter**"). As such, Applicant's amended claim 11 is patentable over the teachings of the **BROOKS** reference.

Further, as noted above, Applicant's amended claim 1 requires the stopping device to issue a stop command to another component, wherein the stop command is provided directly from the stopping device to the other component if the other component is a peripheral (which is patentable over **BROOKS**, as discussed in connection with claim 11) or **selectively, if the other component is a further program operation unit**. Support for the **stop command** (i.e. BRK1) being provided selectively to

a further program operation unit is shown above, and in the instant application, page 12, lines 8 - 14, which states:

> "On their way to the OCDS modules for which they are intended, the signals BRK1 and BRK2 pass through the stopping configuration apparatus CONF. **The stopping configuration apparatus CONF contains switching elements via which it is possible to select whether the signal BRK1 is passed on to the second OCDS module OCDS2, and/or whether the signal BRK2 is passed on to the first OCDS module OCDS1.**" [emphasis added by Applicant]

BROOK specifically teaches in col. 5, lines 51 - 65, that:

> "The features of the microprocessor 102 can be utilized to advantage in a multiprocessing environment. To further illustrate the advantages of the microprocessor 102 in a multiprocessor system 100 in accordance with the present invention refer now to FIG. 3. **As is seen, each of the microprocessors 102 have a common stop pin 112 (i.e., CheckStop.sub.--pin) which changes state based on an active signal being provided by one of the microprocessors 102. Hence, since this common stop pin 112 is present on all of the microprocessors 102 and all the microprocessors 102 are hardwired together via their common stop pin 112, all of the microprocessors 102 will quickly enter a restartable stop state if the stop signal is asserted by one of the microprocessors 102 indicating that a restartable stop condition is initiated.**" [emphasis added by Applicant]

As such, in **BROOKS**, it is **impossible** to **selectively** provide a stop command from one "stopping device" to another "program operation unit". **All** of the processors in **BROOKS** are **hardwired together by their stop pins 112** to ensure that they **all stop as quickly as possible.** To "**selectively**" provide the stop command from the stopping device to a processor of **BROOKS**

would absolutely destroy the teachings of the **BROOKS** reference.

As such, the **BROOKS** reference neither teaches, nor suggests, all of the limitations of Applicant's claimed invention, as set forth above, and in the previous Office Action Response. The **HENNESSY** reference neither teaches the limitations of Applicant's claims that are missing from **BROOKS**, nor, even if it did, would it be combinable with **BROOKS** without destroying the specific teachings of the **BROOKS** reference.

It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of claims 1 and 11. Claims 1 and 11 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claims 1 or 11.

In view of the foregoing, reconsideration and allowance of claims 1 - 17 are solicited.

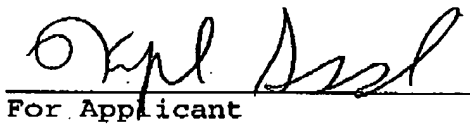
In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out. In the alternative, the entry of the amendment

is requested, as it is believed to place the application in better condition for appeal, without requiring extension of the field of search.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,



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